UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/830,217	04/23/2004	Parthasarathy Ranganathan	200403365-1	9027

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EXAMINER
CONNOLLY, MARK A

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 09/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>23 April 2004</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-34</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1,2,4,5,12,13,16,18,21-27,29,30 and 34</u> is/are rejected.

7)☒ Claim(s) <u>3,6-11,14,15,17,19,20,28 and 31-33</u> is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some *   c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date <u>2/7/06</u>.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1.   Claims 1-34 have been presented for examination.

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this
> or a foreign country, before the invention thereof by the applicant for a patent.

3.   Claims 1-2, 12-13, 16, 18, 21-23, 25 and 29-30 are rejected under 35 U.S.C. 102(a) as

being anticipated by Orenstien et al. [Orenstien] US Pat No. 6804632.

4.   Referring to claim 1, Orenstien teaches the method of selecting I/O devices to control

power consumption of a computer system comprising:

        a.   determining a power consumption metric for each of a plurality of I/O devices

connected to the computer system [col. 3 lines 10-11, col. 4 line 67- col. 5 line 4].

        b.   selecting at least one of the plurality of I/O devices based on the determined

power consumption metric [col. 5 lines 16-20].

        c.   reducing power consumption of the at least one selected I/O device [col. 7 lines 5-

8].

5.   Referring to claim 2, Orenstien teaches a processing unit with very high power

consumption moves its high power process or swaps its high power process with a low power

process thus reducing the processing units power consumption [col. 5 lines 16-20, col. 7 lines 5-8

and col. 8 lines 41-43].

6.   Referring to claim 12, Orenstein teaches the power consumption metric, which is used to

select a processing unit may comprise both a power consumption value and operational activity

[col. 3 lines 17-27].

7.   Referring to claim 13, Orenstein teaches determining an aggregate power consumption

[col. 6 lines 46-54].

8.   Referring to claim 16, Orenstein teaches identifying a setting specifying a constraint with

one of the plurality of devices and reducing the power consumption if the constraint cannot be

maintained [col. 1 lines 6-18].

9.   Referring to claim 18, Orenstein teaches a power consumption metric for each I/O device

comprising an operational activity, which is obtained from polling the I/O devices, is used to

select a processing unit [col. 3 lines 17-50].

10.   Referring to claim 21, Orenstein teaches profiling power consumption of the devices, and

generating a model in which to use in selecting one of the devices [col. 5 lines 16-20].

11.   Referring to claims 22-23, 25 and 29-30, these are rejected on the same basis as set forth

hereinabove.

Claim Rejections - 35 USC § 103

12.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

13.   Claims 4-5, 24-25 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Orenstein as applied to claims 1-2, 12-13, 16, 18, 21-23, 25 and 29-30 above, and further in view

of Cai US Pat No 6501999.

14.   Referring to claim 4, although Orenstein teaches the invention substantially above, it is

not explicitly taught to identify low-power alternatives to using the top power consuming

devices. In summary, Orenstein does not explicitly teach using lower power devices in place of

higher power consuming devices in order to reduce power consumption. Rather, Orenstein

teaches a means in which a processor can be throttled [col. 6 lines 46-54]. Cai teaches a system

comprising a plurality of processors, each with different power consumption levels wherein a

lower power processor is selected to execute instead of a higher power processor in order to

reduce power [col. 1 lines 41-54]. It would have been obvious to one of ordinary skill in the art

at the time of the invention to modify Orenstein to substitute a lower power processor for use

instead of a higher power processor instead of throttling in order to further reduce power as

taught in Cai [col. 1 lines 32-54].

15.   Referring to claim 5, Cai teaches placing a top power consuming I/O device in a low

power mode [col. 3 lines 55-58].

16.   Referring to claims 24 and 25, these are rejected on the same basis as set forth

hereinabove.

17.   Referring to claim 34, Orenstein teaches determining power consumption metrics for

each of a plurality of I/O devices as shown above. Orenstein further teaches operating only one

processor "when battery power falls below a selected threshold" [col. 8 lines 2-6]. Cai teaches

using the lowest power processor during a battery-operating mode allows for extended operating

time [53-58]. It is obvious that the Orenstein-Cai system would examine the power consumption of each processor and select only the most adequate power efficient processor to execute when the battery falls below the threshold. Since only the power efficient processor is executing, it is interpreted that the other processors are in a reduced power consumption state.

18.   Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Singh et al [Singh] US Pub No 2003/0147369.

19.   Referring to claim 26, Singh teaches a means for identifying a plurality of low-power alternative means to using an I/O device connected to a computer system using a usage model and for selecting at least one of the low-power alternative means to reduce power consumption of the computer system [0395]. In particular, Singh teaches the need for encrypting data with a processor in which one of a plurality of encryption levels is selected based on the available power. Although not explicitly taught, it is obvious the system would be able to decipher the power consumption levels associated with each encryption level to ensure that excess power is not being consumed.

20.   Referring to claim 27, the processor encrypting data at a first encryption level and a processor encrypting data at a second encryption level is interpreted as providing substantially the same functionality since both encrypt data.

Allowable Subject Matter

21.   Claims 3, 6-11, 14-15, 17, 19-20, 28 and 31-33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

22.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark Connolly whose telephone number is (571) 272-3666. The examiner can normally be reached on M-F 8AM-5PM (except every first Friday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on (571) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Mark Connolly
Examiner
Art Unit 2115

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mc
September 13, 2006

CHUN CAO
PRIMARY EXAMINER